Unified Design Standard for High-Speed, Mission-Adaptive Avionics Development Platforms

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The development of mission-specific avionics has always been impeded by the need to create custom development platforms tailored to the specific mission requirements, which is both cost and time consuming. This paper proposes a mission-adaptive electrical hardware development environment, presenting a paradigm shift towards a modular and scalable design architecture modeled after the high-speed hardware development processes used in the leading technology sectors. The core of this design standard is the breaking down of avionics systems into a Main LogiC Board and daughter cards that conform to a strict mechanical form factor and a precise electrical pinout specification, which is defined in this work. This specification provides a predictable environment for signal integrity and power conversion by allocating specific pinouts to reduce thermal dissipation and electromagnetic interference. To provide compatibility with a wide range of communication protocols and logic levels, the platform incorporates advanced level-shifting circuits and employs controlled impedance traces on an optimized PCB layer stackup. At the core of the platform's flexibility is a "Smart Motherboard" with a programmable power delivery network that includes high efficiency switching regulators and an intelligent signal traffic network. By taking advantage of high-speed programmable crosspoint switches that are controlled by the onboard microcontroller, the MLB is able to reconfigure the data paths and bus connections between the daughter cards in real-time. To complement this hardware, there is a specialized software library that has been developed as an embedded framework to manage complex signal traffic. This software-defined hardware enables the seamless adaptation of the development platform to a wide variety of mission requirements, effectively decoupling the functional logic of individual subsystems from the physical routing constraints of the PCB. By setting the standard for form factors and pinouts, this paper offers a high-performance, extensible framework that is applicable to rapid prototyping in collegiate research as well as industrial-grade avionics development.

Nomenclature

ADC	=	Analog-to-Digital Converter
DAC	=	Digital-to-Analog Converter
DRC	=	Design Rule Check
EMI	=	Electromagnetic Interference
$HITL$	=	Hardware-In-The-Loop
$HSIO$	=	High-Speed Input/Output
I	=	current
$I2C$	=	Inter-Integrated Circuit
$JTAG$	=	Joint Test Action Group
$LSIO$	=	Low-Speed Input/Output
MLB	=	Main Logic Board
MUX	=	Multiplexer
OTA	=	Over-The-Air
PCB	=	Printed Circuit Board
PMU	=	Power Management Unit

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PWM	=	Pulse Width Modulation
$QSPI$	=	Quad Serial Peripheral Interface
$SMPS$	=	Switched-Mode Power Supply
$SPARC$	=	Scalable Platform for Avionics Routing and Control
$SPARCOS$	=	Scalable Platform for Avionics Routing and Control Operating System
SPI	=	Serial Peripheral Interface
t	=	time
$UART$	=	Universal Asynchronous Receiver-Transmitter
USB	=	Universal Serial Bus
V	=	voltage

I. Introduction

The development cycle for mission-specific avionics systems[1], such as sounding rockets, collegiate-level aerospace projects, or even industrial-strength aerospace projects, typically begins with the development of custom electrical hardware. This traditional method is necessarily inflexible in nature. It is necessary for engineers to design, layout, and develop custom printed circuit boards (PCBs) that meet the specific needs of the mission at hand. Therefore, any modification in the mission requirements or the need to conduct iterative hardware-in-the-loop (HITL) tests for the system or any of the systems involved necessarily requires the redesign of the entire system. This tight integration between the logic of the functional system blocks and the physical constraints imposed by the layout of the avionics PCB is necessarily a major bottleneck in the development cycle for the system at hand.

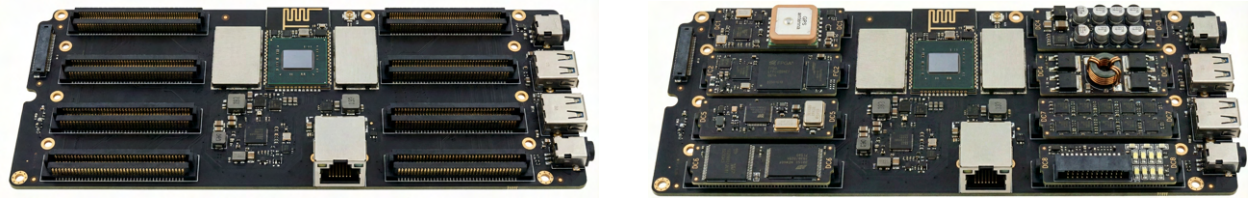
In order to facilitate rapid prototyping and enhance system flexibility, there is a pressing need to design a modular hardware architecture that enables the logical partitioning of avionics systems to be separated from the physical partitioning. Although software-defined architectures have transformed other technology sectors, the hardware sector in avionics has remained rigid in terms of architecture. This paper describes a paradigm shift in the design of avionics systems with the Scalable Platform for Avionics Routing and Control (SPARC) architecture. SPARC is a mission-adaptive electrical hardware development platform that comprises a standardized "Smart Motherboard" (Main Logic Board, or MLB) and Daughter Cards (DCs). By specifying a strict mechanical form factor and a generic electrical pinout as per the APM6 standard, this architecture facilitates plug-and-play modularity.

The core element of the SPARC system is the dynamic signal traffic network. The MLB is able to dynamically reconfigure the data path and bus connections between the daughter cards in real-time through the use of the high-speed programmable crosspoint switches and the dedicated routing controller. The reconfigurability is achieved through the use of the fully custom software library called SPARCOS. The library enables systems engineers to dynamically remap complex communication topologies such as SPI, I2C, UART, and PCIe without the need to modify the physical PCB traces. The SPARC system is further enhanced with an intelligent multiphase power delivery network and continuous wireless telemetry for HITL debugging. The development of the aforementioned design standard will ensure the development of a high-performance system that will greatly reduce development cycle time and costs in both collegiate research and industrial avionics development.

II. Overview of the Development Platform

The development platform consists of two board classes: a main logic board (MLB), depicted without and with daughter cards in Fig. 1a and Fig. 1b respectively, and interchangeable daughter cards (DCs), of which Fig. 2 is an example. Although a highly self-contained architecture was a major requirement, user-defined expandability has been retained in that daughter cards can have a wide range of designs that interface into a standardized mechanical (form factor), electrical, and protocol environment.

The infrastructure provided by the MLB includes multiple regulated voltage rails that accommodate a wide range of power requirements, 20 HSIO connector sets, and crosspoint switches that provide low latency and low distortion signal routing. The daughter cards provide mission-specific avionics functions, of which some examples are sensor interfaces, embedded computing, and high current switching for pyrotechnic ignition. The daughter cards have a common pinout, making all connectors interchangeable, and inter-card communication is provided by the crosspoint switch fabric. The MLB is verified independently using known-good daughter cards; hence, if inter-card communication problems are experienced during integration, they can be definitively diagnosed as due to daughter cards, their configuration, or crosspoint routing and not due to the hardware itself.



(a) MLB Without Daughter Cards (b) MLB With Daughter Cards

Fig. 1 Main Logic Board (MLB) configurations shown separately and with daughter cards installed.

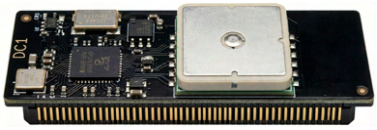


Fig. 2 GPS Daughter Card

III. MLB – Logic

A. Board Routing Controller IC

The Routing Controller IC serves as the central nervous system of the development platform, which runs the Scalable Platform for Avionics Routing and Control Operating System (SPARCOS) software. Given the nature of the SPARCOS, which is designed to allow for easy testing, the primary purpose of the Routing Controller IC is the dynamic configuration of the onboard high-speed crosspoint switch matrix, as illustrated in Fig. 3.

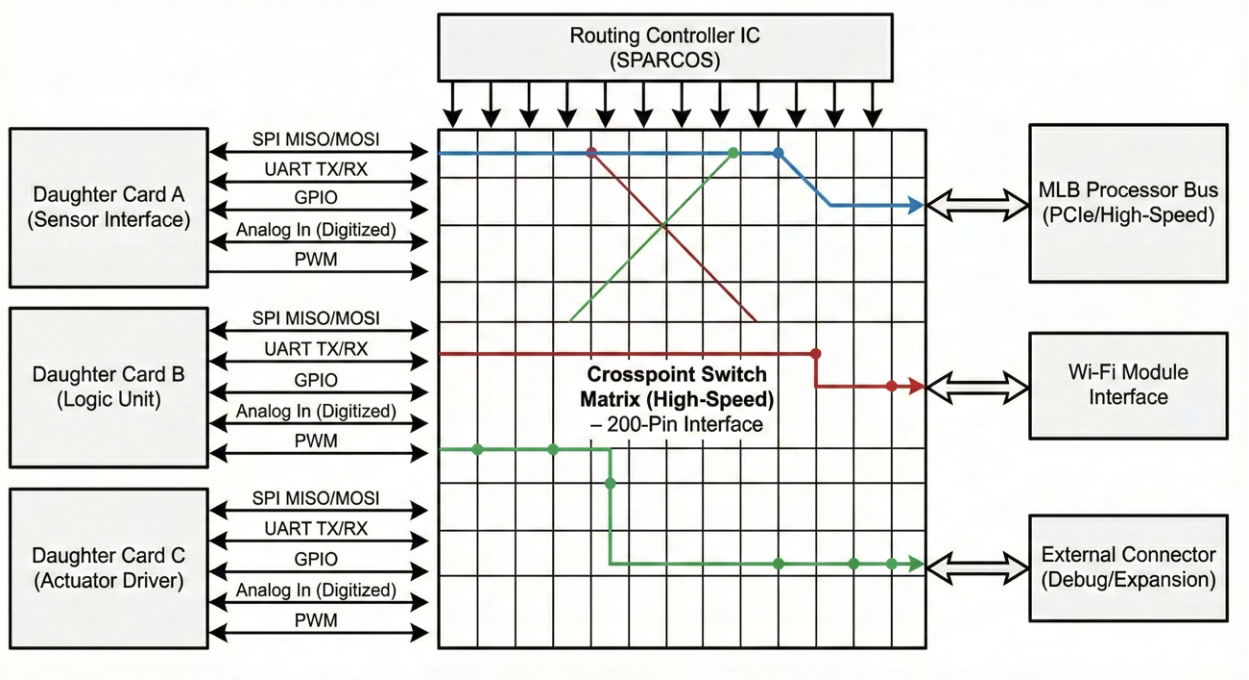


Fig. 3 Example Crosspoint Switches Working Diagram

This decoupling of the logical connections from the physical PCB traces allows the developer to remap buses or different communication topologies without the need to make hardware modifications to the MLB. To ensure the ease of interaction with the system, the routing controller also interacts with the user-developed PC-based configuration user interface.

B. Board Power Monitor Module

In order to provide the necessary environment for the development process, where the experimental or prototype daughter card can be implemented, the MLB has incorporated a dedicated Board Power Monitor Module. This supervisory microcontroller is designed to ensure the electrical integrity and safety of the entire test environment. It is constantly accumulating telemetry data from various distributed current sense amplifiers, voltage dividers, and various precision temperature sensors that are strategically positioned on the board (Fig. 4).

In this way, the real-time thermal telemetry data is correlated with the instantaneous current draw, and the entire profile of the system-wide power consumption and localized thermal effects during the high-load test conditions is provided. When a fault is detected, such as the overheating of various components on the newly developed daughter card, or even the fault in the power delivery network itself, the monitor IC will perform a series of stringent fault handling routines.

The monitor IC is actively engaged in the management of the DC-DC module with the aim of optimizing the delivery of power. It throttles the multiphase buck converters with the aim of validating the models of power efficiency and thermal dissipation under different flight loads.

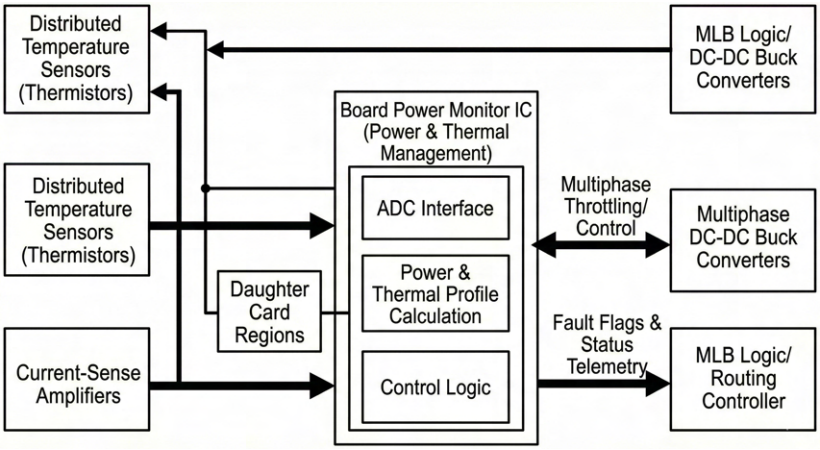


Fig. 4 Board Power Monitor IC Feedback Loop Diagram

C. Wireless Telemetry and Remote Configuration

In order to utilize the SPARC system as a rapid prototyping tool, a high-bandwidth Wi-Fi transceiver module has been integrated into the Main Logic Board. For a typical avionics system development, a means of debug probe attachment is a hardwired JTAG or a UART-to-USB adapter. This is a typical way of system development and is well-suited for a benchtop environment. The drawback of this approach is that physical constraints inhibit system mobility, introduce a potential for a ground loop, and make system testing difficult once the system hardware has been integrated into a vehicle airframe, avionics bay, or environmental test chamber (i.e., thermal vacuum or vibration table test chamber). The SPARC wireless system, shown in Fig. 5, eliminates all of these physical constraints and allows for unencumbered system remote access. Through this wireless interface, the systems engineer is able to interface with the Routing Controller IC and update or network reconfigure OTA. The systems engineer is able to instantly remap the crosspoint switch matrix utilizing a PC-based SPARCOS graphical interface without physically interacting with the hardware.

Moreover, the Wi-Fi module is employed as a different route for the real-time system diagnostics, which is independent of the main flight computer's telemetry. It is always broadcasting real-time board-level health indicators such as localized temperature maps, power rail currents, and automatic fault indicators provided by the Board Power Monitor IC. This remote accessibility is highly advantageous for the Hardware-In-The-Loop (HITL) simulation, where it is necessary to monitor the power characteristics, routing faults, and system redundancy.

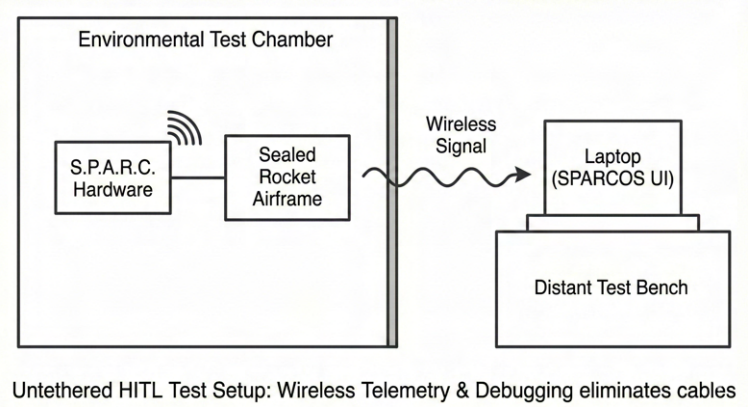


Fig. 5 Controlling SPARC Through Remote SSH and SPARCOS

IV. MLB – Power

A. Power Management Unit

Since the MLB provides multiple, configurable power rails via dedicated regulators, it is laid out to support a wide range of operating voltages while minimizing conversion losses through high-efficiency power-stage design, as shown in Fig. 6. The PMU supports diverse voltage and current requirements and provides the user with both digital telemetry and analog feedback for monitoring power consumption.

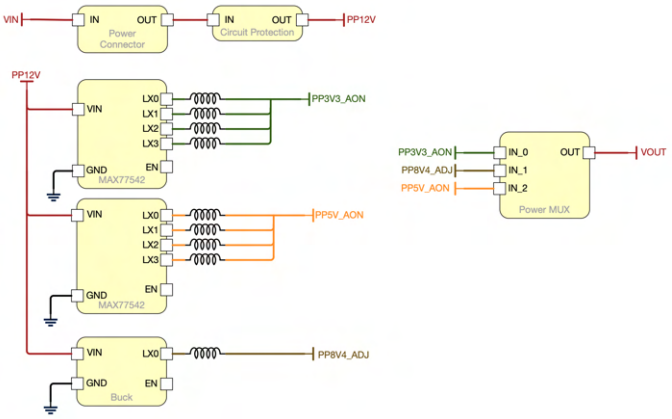


Fig. 6 Simplified PMU System Architecture Diagram

1. Voltage Regulator Choice

We designed the DC–DC module to deliver up to 490 W while minimizing conversion losses to conserve onboard battery energy. We rejected linear step-down regulators (e.g. LDOs) because they regulate with a series pass element and dissipate the input–output voltage difference as heat, which severely reduces efficiency at high load power. Instead, we selected a SMPS buck-converter topology to achieve high conversion efficiency (>92%) over the required operating range. We ultimately selected a multiphase buck converter due to the benefits described in IV.A.2.

2. Multiphase Buck Converters

Despite their efficiency advantages, single-phase buck converters present several practical drawbacks. High switching frequencies produce large dv/dt and di/dt at the switching node, which generate EMI; we address this issue in Sec. IV.B. Buck-converter ICs can overheat and degrade system performance; we discuss the corresponding layer-management and thermal-design considerations in [2]. In addition, the LC output network introduces ripple, and reducing that ripple

often worsens the transient response by requiring larger inductance values.

We selected a multiphase buck-converter architecture to mitigate these limitations. A multiphase converter interleaves several power stages, each with its own inductor, at a common regulated output. By phase-shifting the switching waveforms, the converter causes partial cancellation of the inductor ripple currents (Fig. 7), which reduces output ripple and improves EMI performance [3]. For each phase, the ripple current follows

$$\Delta I_L = \frac{(V_{in} - V_{out})D}{L f_{sw}}, \qquad D = \frac{V_{out}}{V_{in}}, \tag{1}$$

which yields

$$L = \frac{(V_{in} - V_{out})V_{out}}{\Delta I_L f_{sw} V_{in}}. \tag{2}$$

Because the converter shares the total load current across phases,

$$I_{phase} = \frac{I_{total}}{n}, \tag{3}$$

each phase carries less current, which allows smaller per-phase inductance values while maintaining acceptable ripple. This current sharing also improves load-transient response by reducing output-voltage droop during rapid load steps. We therefore chose a multiphase buck-converter architecture to reduce ripple, improve EMI behavior, and enhance transient performance.

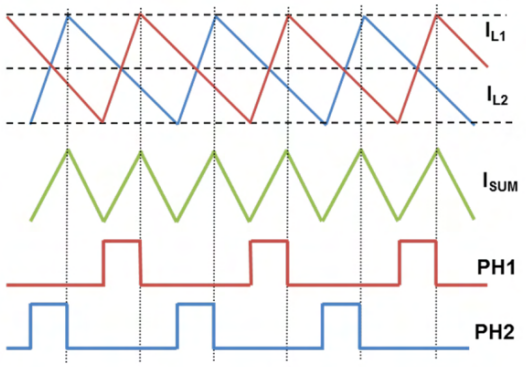


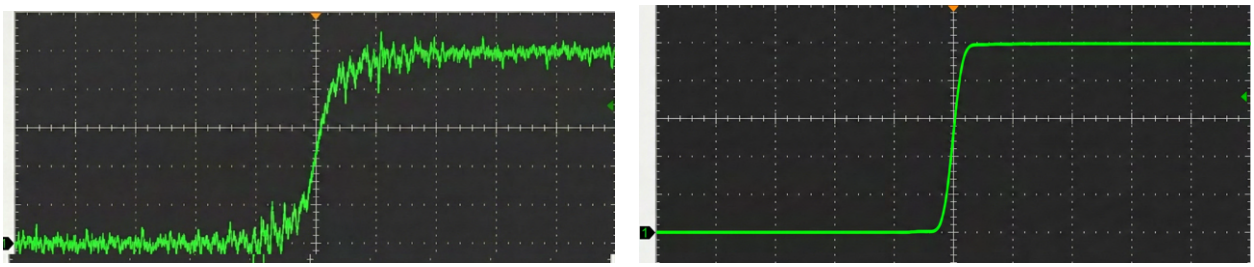
Fig. 7 Phase ripple current cancelling each other out. Image used courtesy of Texas Instruments

B. EMI Shielding

However, controlling the propagation of the electromagnetic field in the PCB is vital in avoiding parasitic coupling. Electromagnetic interference (EMI) is particularly harmful in HSIO interfaces because the fast transition times produce wideband noise that reduces the receiver timing margin. Fig. 8a shows the degradation in the quality of the edges of the signal caused by inadequate shielding compared to the well-controlled edges in Fig. 8b.

Our design team uses the following techniques in the design of the PCB to limit the effects of EMI:

- *Continuous return planes:* Using continuous ground planes placed adjacent to the signal layers is vital in the design of the PCB. The continuous ground planes provide return paths that couple the electromagnetic field to the return plane. The continuous return path reduces crosstalk effects.
- *Isolate aggressors and victims:* We isolate the aggressors from the victims using physical separation techniques. The aggressors contain the noisy signals, while the victims contain the sensitive signals.
- *Optimized layer stackup:* We partition the HSIO, LSIO, power, and GPIO routing domains in the design of the PCB as shown in Fig. IV.C. Routing the HSIO signals between the solid ground planes mitigates interference and crosstalk.



(a) Degraded edge due to poor EMI shielding **(b) Ideal controlled edge**

Fig. 8 Comparison of signal edge fidelity with and without adequate EMI shielding.

C. Layer Stackup

For the MLB stackup, we selected a six-layer board in which each layer serves a specific function, Fig. 9 depicts the layer ordering visually:

- *L1–L3:* We use the first three layers primarily for low-speed I/O (LSIO) routing. We route most power planes on Layer 1 to reduce the total number of power vias and thereby limit via current density, IR drop, and localized heating.
- *L4:* We dedicate Layer 4 to a solid ground plane that isolates the LSIO victim nets from the HSIO aggressor nets.
- *L5:* We route all high-speed I/O (HSIO) signals on Layer 5 and intentionally separate them from LSIO routing for the EMI-control reasons discussed in Sec. IV.B.
- *L6:* We dedicate Layer 6 to a second solid ground plane that shields the HSIO layer from external interference and helps contain radiated emissions from the board.

Top Solder Mask	1.000 mil	Solder Mask
Top Surface Finish	0.787 mil	Surface Finish
L1	1.377 mil	HSIO
Dielectric	3.913 mil	FR-4
L2	0.598 mil	GND
Dielectric	21.655 mil	FR-4
L3	0.598 mil	LSIO
Dielectric	4.284 mil	FR-4
L4	0.598 mil	Power
Dielectric	21.655 mil	FR-4
L5	0.598 mil	GND
Dielectric	3.913 mil	FR-4
L6	1.377 mil	HSIO
Bottom Surface Finish	0.787 mil	Surface Finish
Bottom Solder Mask	1.000 mil	Solder Mask

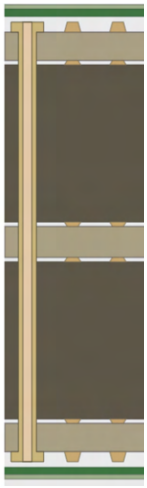


Fig. 9 MLB stackup

D. Expansion Capabilities

To enhance system versatility, MLB includes an Ethernet port, enabling potential integration with additional computing units. This feature allows for expanded connectivity options and provides flexibility for future development and testing scenarios requiring networked communication between multiple systems.

V. Daughter Card Design Standards

To guarantee true modularity and mission adaptability, all user-designed daughter cards must comply with a strict set of design standards. From a mechanical standpoint, the daughter card is constrained to a precise 3x2 inch format. The high-speed mezzanine connector is placed along one edge of the board, while the opposite edge contains two standardized bosses for secure screw mounting to the MLB, thereby ensuring rigidity.

The physical interface to the MLB is implemented via the Samtec AcceleRate® HP High-Density Array connector. The MLB contains the female connector (APF6 series), while all daughter cards must use the mating male terminal with the part number APM6-060-X-X-04-0-A-X. With its ultra-compact 0.635 mm pitch open-pin-field design, the connector supports data rates up to 112 Gbps PAM4 while remaining fully compatible with the PCIe 6.0 and 100 GbE standards. The connector terminates via a robust solder column board termination that provides excellent mechanical retention while offering maximum routing flexibility. To prevent crosstalk while keeping sensitive signals separate from noisy power connections, the 200-pin interface is strictly segmented into four distinct functional domains.

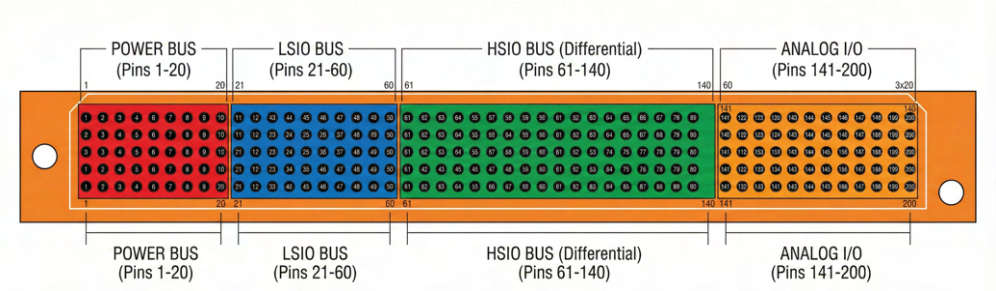


Fig. 10 APM6-60 Standardized Daughter Card Pinout

A. Power Bus

Pins 1 to 20 of the APM6 connector are entirely reserved for power distribution and return grounds. As the power requirements of the daughter cards vary greatly, ranging from 3.3V logic for sensor payloads to 8.4V for pyrotechnic deployment systems, the MLB makes use of an intelligent Power Multiplexer (MUX) system. To configure the voltage rails for a specific slot, the Power MUX can be set in two different ways: through manual configuration using DIP switches placed adjacent to each daughter card slot of the MLB, or through software control using the Board Routing Controller IC.

B. Single Ended LSIO Bus

Pins 21 to 60 of the APM6 connector are reserved for the Single Ended Low Speed Input/Output Bus. This bus domain deals with standard communication protocols for embedded systems, including UART, I2C, standard GPIO, and low-frequency Pulse Width Modulation signals. As the signals are of low frequency, standard digital crosspoint switches are used for routing the LSIO Bus signals across the MLB. To ensure compatibility across different types of microcontrollers and ICs, daughter cards are required to have onboard level-shifting circuits for logic voltage levels other than the standard 3.3V logic voltage supplied by the MLB.

C. Differential Pair HSIO Bus

The High-Speed Input/Output Bus, which spans from pin 61 to 140, is dedicated to handling bandwidth-intensive protocols such as Ethernet, USB, and high-speed QSPI. It bypasses the standard logic switches and utilizes high-bandwidth differential crosspoint switches.

1. Impedance Profiles

For the smooth passage of the signal from the MLB to the daughter card without any reflection or attenuation, the daughter card must adhere to the impedance profiles defined on the MLB. Instead of forcing the daughter card to adhere to one single standard for the entire HSIO Bus, the MLB routes the high-speed interface across different lanes, each of which is designed with different characteristic impedances. For example, the MLB has lanes dedicated to the 90Ω

characteristic impedance for the USB interface, while others are designed for the 100Ω characteristic impedance for the Ethernet interface. It is the responsibility of the designer of the daughter card to map the high-speed interface to the appropriate lane, maintaining the impedance profile by matching the trace width and dielectric spacing for the APM6/APF6 interface.

2. Signal Integrity Mitigation

In addition to good impedance management, daughter card designs must incorporate aggressive signal integrity mitigation techniques. Differential high-speed signals must be length tuned to match propagation delays and minimize phase skew between the positive and negative signals. During length tuning of these differential signals, it is important to note the requirement to maintain a strict maximum uncoupled length to prevent these differential signals from decoupling and causing EMI. In addition to length tuning of differential signals, it is important to note the requirement for HSIO signals to minimize layer transitions. A strict maximum via count requirement must be met for all high-speed signals to minimize parasitic inductance and impedance discontinuity. In cases where vias are unavoidable for length tuning of differential signals and/or for minimizing layer transitions for single-ended HSIO signals, it is important to note the requirement to implement via antipads of proper size to minimize parasitic capacitance and maintain the integrity of the transmission line structure. Finally, it is important to note the requirement to maintain uninterrupted ground reference planes directly beneath all HSIO signals to maintain integrity of these signals by containing electromagnetic fields and preventing crosstalk with adjacent pins.

D. Analog IO Bus

Passing analog voltages through the digital crosspoint switches in the MLB would result in unacceptable levels of parasitic capacitance and signal degradation. As such, the SPARC architecture adheres to a strict boundary-digitization rule for pins 141 through 200. No raw analog signals are routed through the APM6 connector; rather, all analog signals are digitized or reconstructed on the daughter card.

1. DAC Selection

In cases where the daughter card requires analog control signals (for example, when a legacy actuator receives a variable reference voltage or when a proportional valve is driven), the card must contain a Digital-to-Analog Converter (DAC). The MLB transmits the desired voltage level as a digital message through the crosspoint matrix, and the onboard DAC reconstructs the analog signal. The designer must choose DACs with adequate settling time and resolution (usually 12-bit or 16-bit) to satisfy the precision requirements of their actuators without introducing step-change jitter.

2. ADC Selection

On the other hand, when dealing with the acquisition of data from analog sensors such as thermistors, pressure transducers, and strain gauges, the daughter card is required to perform the local digitization using an Analog to Digital Converter (ADC) before the transmission. Therefore, the ADC is located as close to the source of the analog signal as possible, and the EMI traces are kept extremely short. The digitized sensor data is securely transmitted across the APM6 connector and the MLB's digital routing matrix. The selection criterion for the ADC is based on the ability to support high sampling rates and at least 16-bit resolution for the acquisition of high-fidelity flight telemetry, with the ability to support anti-aliasing filters to reject high-frequency noise from the vehicle.

VI. Customized Software Routing Platform (SPARCOS)

SPARCOS consists of the embedded firmware running on the MLB Routing Controller IC and its PC-based graphical user interface. This abstracts the complex hardware layer and enables the dynamic manipulation of the physical architecture of the Avionics stack by the systems engineer using simple software commands rather than soldering and/or wiring.

A. Signal Definition

The primary purpose of SPARC OS is the management of the high-speed crosspoint switch matrices. Through the PC interface, as represented in Fig. 11, the user is provided with a digital version of the 200-pin APM6/APF6 connectors for all populated daughter card slots. It is the developer's task to logically connect the signal by mapping the

Fig. 11 SPARCOS Custom User Interface showing the signal routing matrix, power configuration parameters, and real-time system telemetry.

digital version of one output pin to another input pin on the daughter card. It is during this process that the developer must specifically declare the communication protocol associated with the signal, such as defining the pin as SPI, such as MISO, MOSI, or SCK; I2C, such as SDA or SCL; or UART. This ensures the logical compatibility of the signal, as SPARC OS rigidly defines the communication protocol associated with the signal, preventing the designer from mistakenly routing the signal from one protocol to another.

This process of abstraction means that the complexity of the crosspoint matrix is automatically taken care of by the software as it converts the logical map presented by the user into the actual binary bit streams necessary for the switch ICs. Another feature of the SPARC OS is its management of the domain isolation as specified in the hardware standard, where the LSIO logic definitions are routed via the standard digital matrix while the HSIO definitions are routed via the impedance-matched differential lanes.

B. Bus Contention Verification

As the traces are fully software-defined, there is a potential for user-caused routing errors, such as accidentally connecting two active transmitter (TX) lines together, or directly connecting a high-speed data line to a ground pin. These configurations will cause bus contention, potentially leading to extreme electrical spikes, high current consumption, and destruction of the silicon drivers on the daughter cards.

To address this problem, SPARCOS introduces an automated Bus Contention Verification system. Prior to applying any new routing configuration to the physical crosspoint hardware, the software performs a Design Rule Check (DRC) on the configuration, the status of which is continuously tracked within the user interface. The software examines the proposed signal routes as a directed graph, checking signal orientation and ensuring that every net has exactly one driving source and at least one valid receiver. If a violation or domain boundary error (such as routing an analog pin into the HSIO matrix) is found, the OS prevents the configuration from being applied and notifies the engineer of the particular routing error.

C. Power Configuration

In addition to signal routing, SPARCOS is also the command interface for the MLB's power delivery system. Using the software's power configuration panel (Fig. 11), users can dynamically assign particular regulated voltage rails to the Power Bus (Pins 1-20) of each individual daughter card slot via the Power MUX.

Additionally, the operating system provides the ability for developers to create their own custom power profiles for their testing platform. Users can specify programmable over-current trip points (which can be considered as highly

sensitive software e-fuses), set up under-voltage lockout thresholds, and control the exact startup sequencing and soft-start times for each rail. This is particularly important for simulating different flight states and avoiding the inrush current spikes and power comas that were described in the previous transient analyses.

D. System Health Inspection

For the purpose of rigorous Hardware-In-The-Loop (HITL) testing, the SPARCOS system includes a System Health Inspection dashboard. Using the MLB's Wi-Fi module, the PC interface receives a continuous high-frequency telemetry signal from the Board Power Monitor IC.

The interface aggregates and displays important environmental information, such as the momentary current consumption and voltage levels of all active power rails, as well as a real-time thermal map created by the distributed temperature sensors. By recording this information, developers can link particular software events, such as extreme actuator commands, to their immediate thermal and electrical effects on the hardware. In the event that the telemetry data shows a critical violation of the safety thresholds set during the Power Configuration phase, the SPARCOS system automatically commands the Routing Controller to go into a safe state, turning off the involved modules in order to maintain the integrity of the development environment.

VII. Conclusion

This paper has proposed a conceptual framework for a mission-adaptive avionics development environment, utilizing a standardized Main Logic Board (MLB) and interchangeable Daughter Cards (DCs). At its heart, this paper has proposed a robust hardware protocol, namely a strict mechanical form factor and a universal electrical pinout, that in effect divorces functional subsystem logic from physical constraints of a motherboard. Although this complete and unified architecture is proposed in a conceptual manner, several key subsystems, namely power delivery network, EMI shielding, and basic high-speed I/O routing, have been successfully prototyped and proven. Because of this high degree of flexibility and modularity, this standardized hardware protocol is uniquely well-positioned to significantly enhance rapid prototyping efforts over a broad range of application domains, from collegiate-level avionics design competitions to extremely robust and industrial-strength development environments.

Future work will be centered on increasing the interconnect density of the platform, which is currently limited by the relatively low pin count of existing crosspoint switches. To overcome this physical routing constraint, we are exploring the possibility of developing custom silicon to replace the crosspoint switches, which would greatly expand the signal matrix size. In exploring the possibility of replacing the dynamic signal routing with one of these solutions, FPGAs were considered for the task of managing the dynamic signal traffic network. However, the compilation and flashing turnaround times associated with FPGA development were found to be too great for the type of iterative hardware-in-the-loop testing for which this platform was designed. Moving to custom silicon for dynamic signal routing will allow us to fully realize the vision of a plug-and-play environment for high-speed avionics development.

Acknowledgments

The authors would like to acknowledge the Guidance, Navigation, and Controls project and the avionics subteam at the Georgia Tech Ramblin' Rocket Club for their support throughout the entire development process. Additionally, the authors would like to express their appreciation to the HIVE Makerspace at Georgia Tech for sponsoring the testing equipment used in the hardware bench testing. Lastly, the authors express their gratitude to Mingjie (Jack) Wei and Andrés De La Torre for their support in the system architecture and PCB design.

References

[1] Liu, C., "Active Control and Guidance-Aided Propulsive Landing Research for Small-Scale Vehicles," *2024 Regional Student Conferences*, 2024, p. 83778.

[2] Liu, C., Abdeen, M., and Chugh, K., "Development of a High-Performance Avionics System for Real-Time Guidance and Control in High-Power Vehicles," *2025 Regional Student Conferences*, 2025, p. 99768.

[3] Parisi, C., "Multiphase Buck Design From Start to Finish (Part 1)," , Apr. 2021. URL `https://www.ti.com/lit/an/slva882b/slva882b.pdf`, application Report (revised April 2021).