Development of a High-Performance Avionics System for Real-Time Guidance and Control in High-Power Vehicles

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In recent decades, guided space-shot vehicles have successfully adhered to their preplanned trajectories with the help of advanced state estimation algorithms. However, these algorithms require reliable hardware platforms capable of supporting the high processing speeds necessary for real-time computation. This study aims to explore a system consisting of rigid hardware, including power management, microcontrollers, sensor integration, and telemetry. These systems are intended to be implemented as two Printed Circuit Boards (PCBs), which are modularized based on their functions within the overall system in a 3" × 7" format. The research involves power electronics design and optimization—studying and building energy-efficient circuitry to supply power to the entire onboard electrical system. Because of the use of a high-current actuator system, real-time power monitoring is essential to ensure nominal performance. Due to the rocket's high velocity and short reaction time during flight, high-speed data lines such as SPI, QSPI, and Ethernet are implemented to reduce propagation delay within the electrical system. Additionally, real-time communication with the ground computer provides an essential safety mechanism, allowing mission control to initiate a controlled flight termination if necessary. This study offers valuable insights into high-performance avionics system design through rigorous signal integrity (SI) and power integrity (PI) analysis, culminating in thorough system validation and testing.

Nomenclature

$I(t)$	=	current
$V(t)$	=	voltage
$P(t)$	=	power
Z	=	Impedance
PWM	=	Pulse Width Modulation
SPI	=	Serial Peripheral Interface
$QSPI$	=	Quad Serial Peripheral Interface
USB	=	Universal Serial Bus
EMI	=	Electromagnetic Interference
PCB	=	Printed Circuit Board
$JTAG$	=	Joint Test Action Group
MCU	=	Microcontroller Unit
SD	=	Secure Digital

I. Introduction

Over three decades ago, a conjecture was introduced that predicts the evolution of modern processor capabilities. Known as Moore's Law, it asserts that the processing power of silicon chips doubles approximately every two years. This remarkable progress is fueled by continuous advancements in manufacturing technologies, which enables an

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increasing number of transistors to be packed into each square inch of silicon die[1]. These remarkable advancements in engineering have had a directly impact on the aerospace industry, particularly in the area of flight avionics systems. These systems are essential for controlling the vehicle and ensuring it performs its intended mission with precision and reliability.

Aimed at integrating processing power, high-quality sensor data acquisition, and redundant safety measures into a single compact system, this study was initiated under the Guidance, Navigation, and Control (GNC) program, with the objective of conducting GNC research by developing a jet-vane-controlled rocket powered by an N-Class solid rocket motor. With a vehicle that has a maximum velocity exceeding the speed of sound, the control hardware within the avionics module must be designed around reliability and fast response time to counter any deviations during flight[2]. After a proposed solution, the study will be rigorously carried through comprehensive testing and validation procedures, which is also document in this paper.

II. Overview of the Avionics System

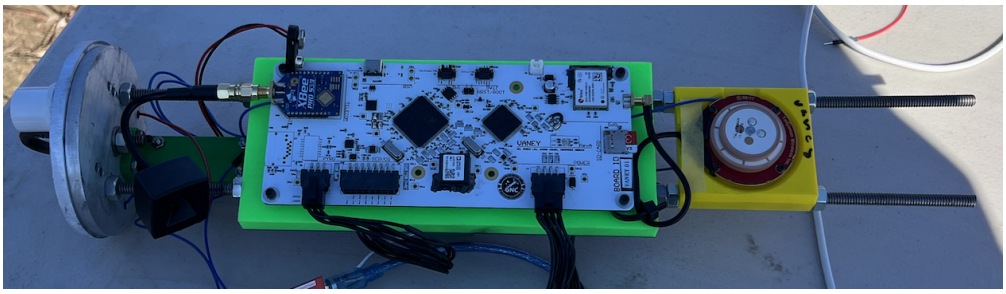


Fig. 1 Avionics system stackup from the high-G testing mission

The avionics system (Fig. 1) is composed of two distinct boards: the Power Management System (PMS) (Fig. 2) and the Flight Computer (Fig. 9). This division of power and logic units is implemented to facilitate easier debugging and troubleshooting, allowing for more efficient identification and resolution of issues during the development and operational phases. Both system are fully tested before the integration, avoiding the incident such as faulty power module causing negative effects on the performance flight computer.

A. Power Management System

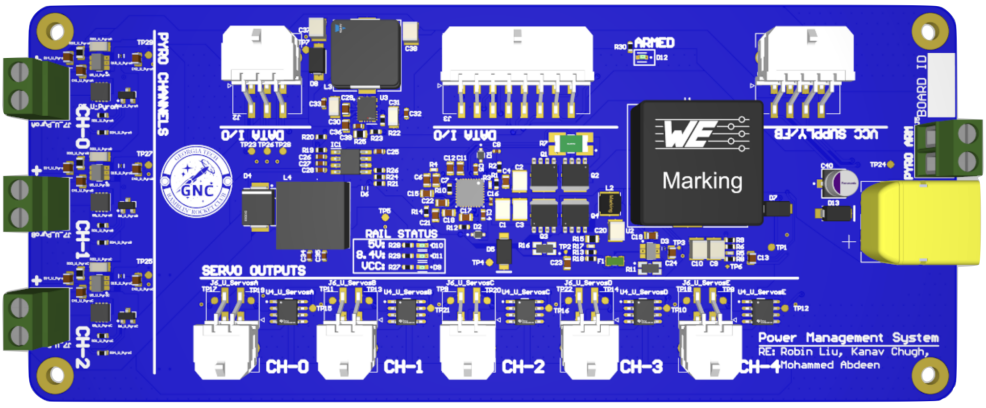


Fig. 2 3D model of the PMS

The PMS is capable of supplying power at various voltages and current requirements, deploying charges across the jet vanes of the rocket, and providing digital and analog feedback on power consumption to the logic unit.

1. Pyrotechnic Module

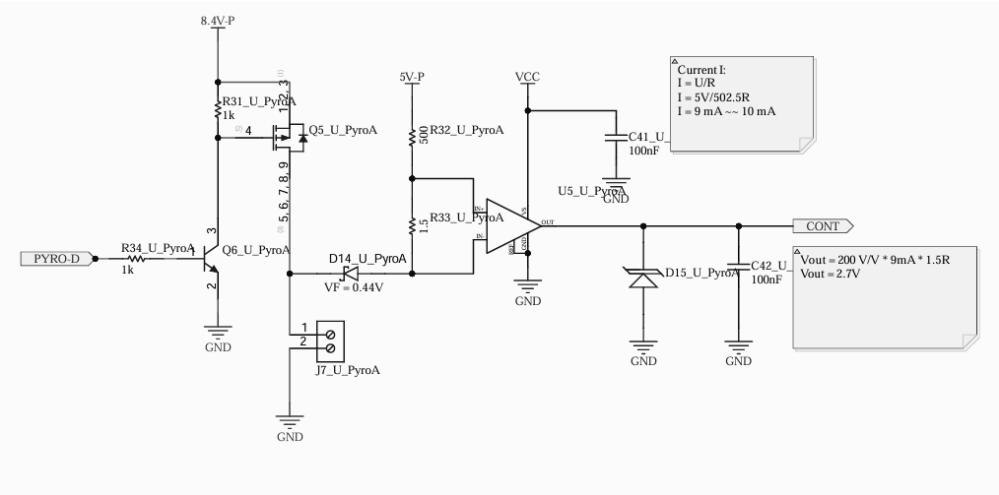


Fig. 3 Schematic capture of the pyrotechnic module

In order to deploy pyrotechnic charges on the rocket, such as the parachute deployment charge, pyrotechnic module on the PMS is engineered to output a large amount of power. Therefore, the circuit is equipped with the capability of supplying 10A at 8.4V. Based on Equation (1), the power of the output channel can be as high as 84W, capable of deploying any Nichrome-fused charges within 5 milliseconds. The pyrotechnic module is controlled by the digital signal sent out by the flight software running on the flight computer. The signal drives the gate of the transistor high, allowing the current to flow through the charge.

$$P(t) = I(t) \times V(t) \tag{1}$$

The pyrotechnic module has additional capabilities, such as continuity sensing. This feature is carried out by applying a minimal voltage across the Nichrome-fused charge without deploying it. By reading the current running through the charge, the flight software is able to determine if the ignition charge is installed correctly.

2. DC-DC Module

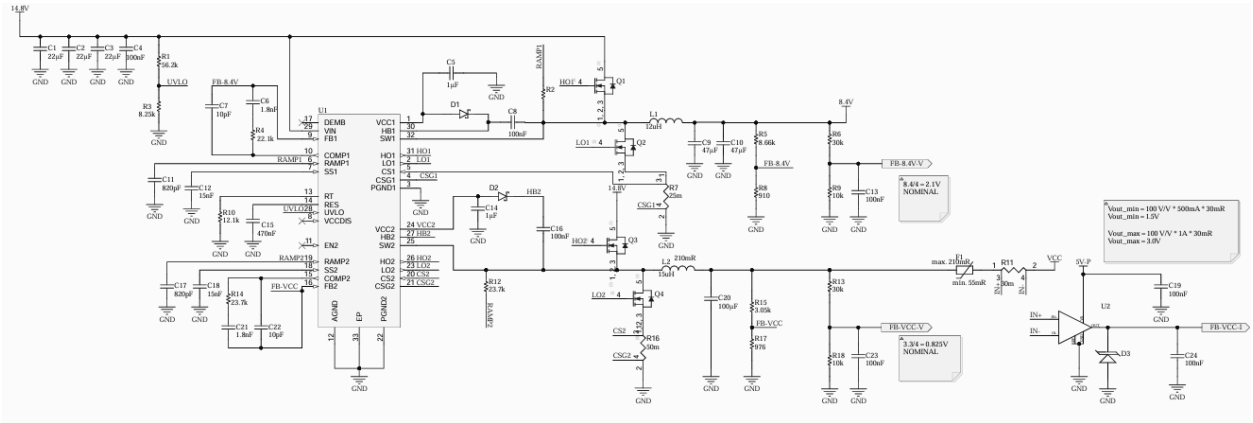


Fig. 4 Schematic capture of the DC-DC module

The DC-DC module (Fig. 4) is responsible for stepping down the source voltage provided by a Lithium Polymer (LiPo) battery to a lower, yet stable, voltage. The circuit operates under the law of conservation of energy, where the voltage is decreased and the current is increased, keeping the overall power constant. The constant oscillation of energy

between an inductor and a capacitor allow the voltage change to occur. Of course, energy conservation works in an ideal environment – there will be a slight loss of energy due to thermal dissipation in real world.

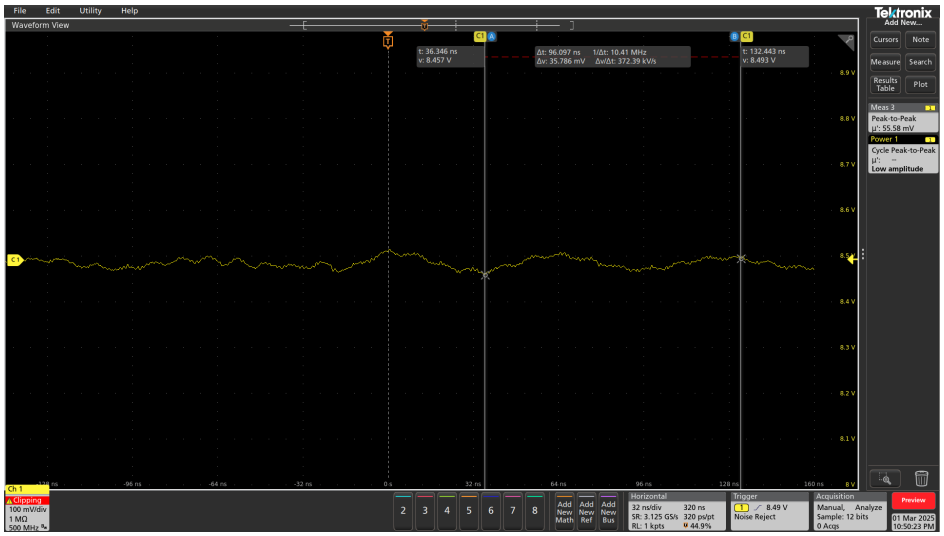


Fig. 5 Oscilloscope capture of nominal output of the DC-DC module

Since the inductor-capacitor (LC) circuit inside the DC-DC module will produce AC component along with the DC power, the module is designed to have minimal ripple voltage/current. Fig. 5 showcases the nominal rippled of 2%.

3. Thermal Performance

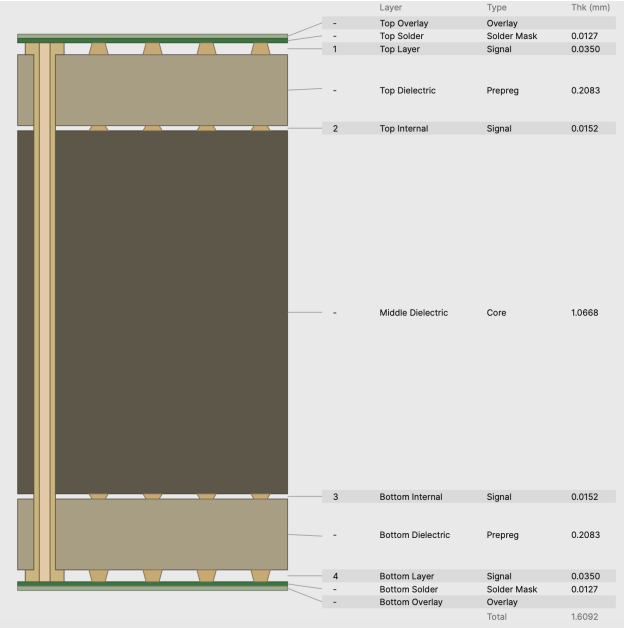


Fig. 6 Layer stackup of the PMS

Heating caused by high current flowing through a trace on the PCB can be detrimental to the performance of the silicon chips. Therefore, effective thermal dissipation is required to reduce heating of the PMS. Since installing any active mechanical cooling device on the PMS would not only add weight to the rocket but also increase the likelihood of failure in a high-vibration environment, PMS applies a passive cooling mechanism by utilizing a specific layer stackup

(Fig. 6) configuration within the PCB. Since the PMS is a 4-layer PCB, we configure the stackup to have two ground copper planes in the middle. As a result, the heat generated by the chips on the top and bottom layers can be dissipated through the two middle copper layers. As shown in Fig. 7, the result of the thermal imaging shows that the temperature of the PMS was greatly reduced, significantly improving the efficiency of the IC.

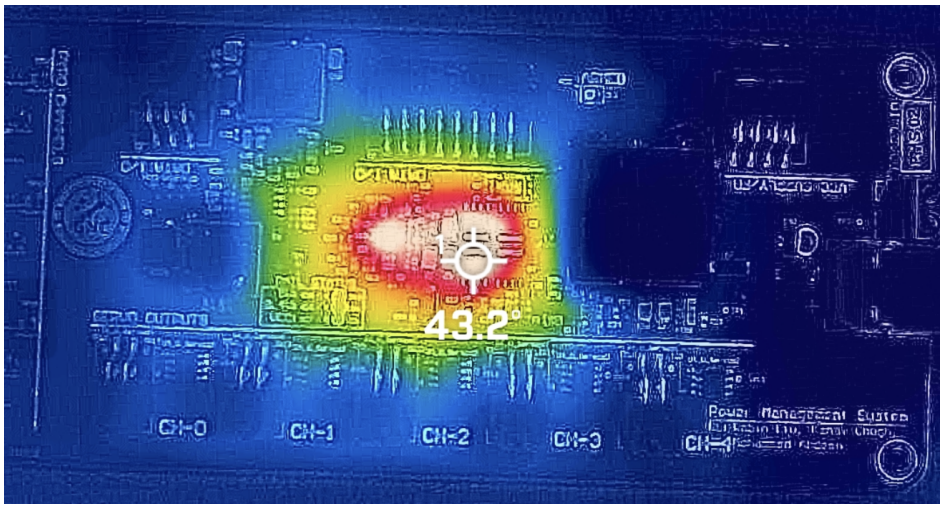


Fig. 7 Thermal imaging of the PMS in its nominal state

4. Real Time Power Monitoring

To verify that the system is functioning correctly both on the launch pad and in the air, the PMS is equipped with accurate Hall Effect sensors that monitor the current consumption on each voltage rail. Fig. 8 illustrates the current sensing within the actuator output channels. The Hall effect sensor converts the current reading into a voltage (analog signal) which is sent to the flight computer.

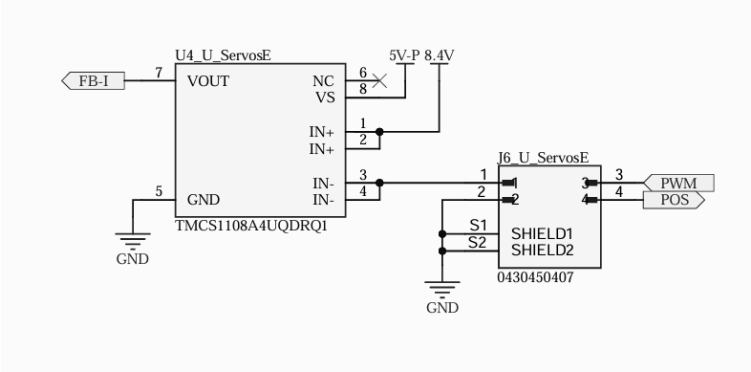


Fig. 8 Schematic capture of the current monitoring module

B. Flight Computer

The Flight Computer (Fig. 9) is responsible for sensor data acquisition, processing, storage, and communication with the ground control station. As the central component of the avionics system, it serves as the main processing unit for flight operations. The flight computer is equipped with two single-core STM32 microprocessors, ensuring high-speed data processing and efficient I/O management across various sensors. The following sections outline key design considerations for both the schematic and physical layout development.

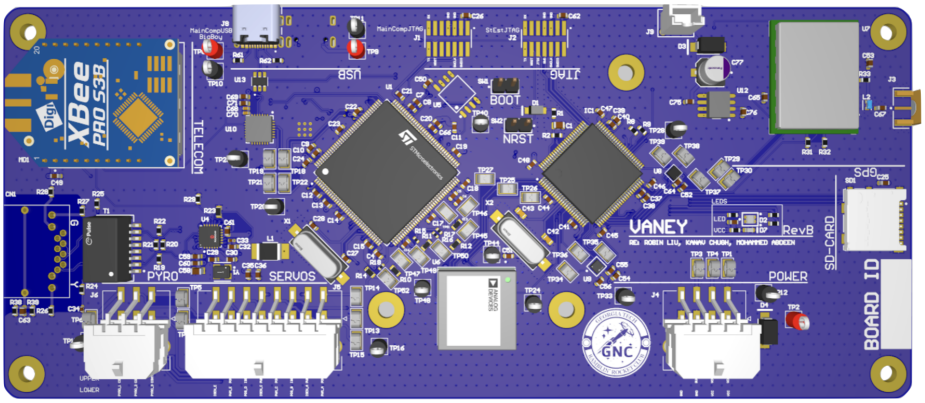


Fig. 9 3D model of the Flight Computer

1. Impedance Matching

Impedance refers to the opposition to alternating current (AC) caused by the combined effects of resistance and reactance [3]. Any time-varying direct current is considered AC in this context. Impedance matching is the process of minimizing impedance differences between the source and the load to ensure signal integrity [4].

Impedance matching is particularly critical in high-speed digital communication systems. Mismatched impedance can lead to drastic fluctuation of voltage, leading to faulty bit reading and reduced system performance. To mitigate this, precise calculations must be conducted.

A common method for analyzing impedance is to model PCB copper traces as transmission lines (an array of infinitesimal inductors and capacitors [4]). The total impedance of the transmission line is then determined using Equation (2). In real world application, source and load impedance are known, while the transmission line impedance must be calculated.

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{2}$$

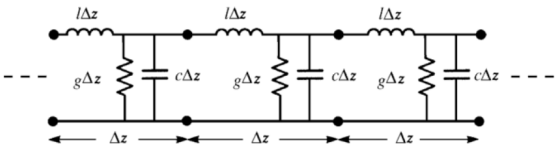


Fig. 10 Model of transmission lines as inductors and capacitors

2. Physical Layout Considerations

Impedance constraints must be incorporated into the physical layout, where most signal transmission occurs via microstrip traces.

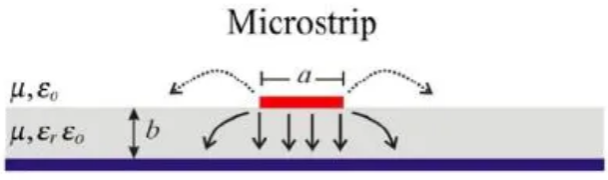
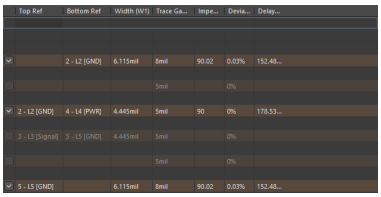


Fig. 11 Cross sectional view of a microstrip (red)

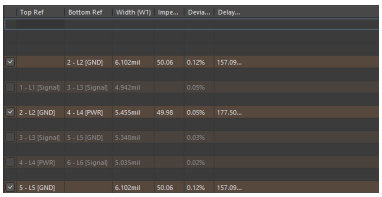
Using the microstrip model in Fig. 11, the characteristic impedance is calculated as using equation (3) where a is the trace width, b is the distance to the closest reference plane, and $a < b$.

$$Z_0 = \frac{1}{2\pi}\sqrt{\frac{\mu}{\epsilon_f}}\ln\left(\frac{8b}{a} + \frac{4a}{b}\right), \tag{3}$$

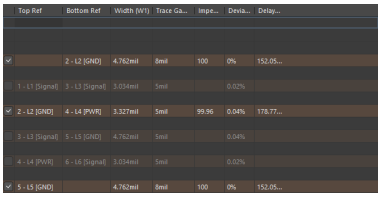
The required impedance value depends on the communication protocol being implemented. In general, a 50Ω impedance is widely used as a balance between signal integrity and power loss for protocols such as SPI and QSPI. For higher frequency protocol such as USB and Ethernet, standardized values of 90Ω and 100Ω are used, respectively.



(a) 50Ω impedance profile



(b) 90Ω impedance profile



(c) 100Ω impedance profile

For differential pairs, mirrored signal traveling close to each other, the trace gap must also be considered when achieving appropriate impedance. Using manufacturer-provided values for the reference plane distance showned in Fig. 13, the necessary trace widths and gaps are determined to achieve the target impedance for the flight computer's high-speed communication buses.

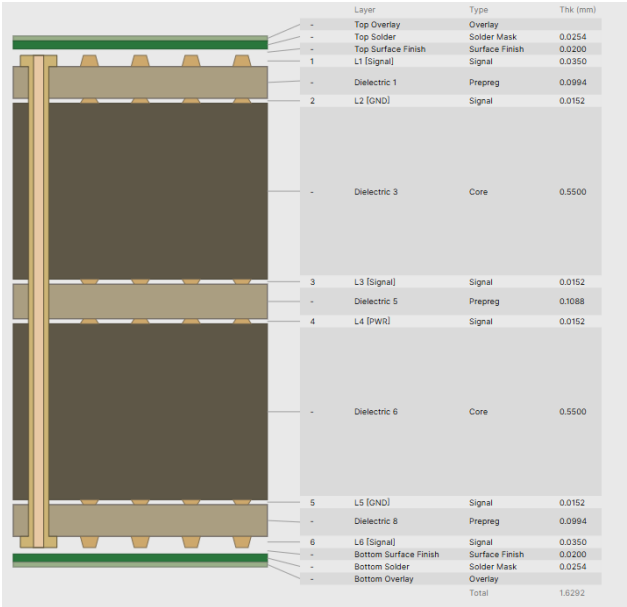


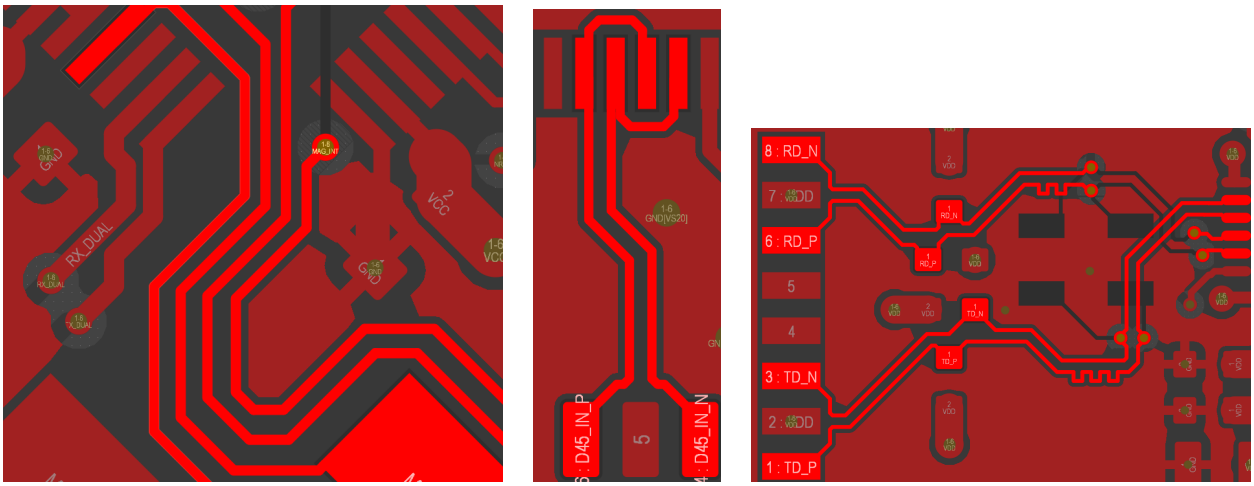
Fig. 13 Flight Computer layer stackup

3. Signal Routing Considerations

As the flight computer circuitry is implemented on a PCB, proper signal routing is crucial to ensure reliable operation. The primary high-speed communication buses include SPI, USB, and Ethernet, with numerous traces carrying analog voltage and PWM signals. Given their sensitivity to electromagnetic interference (EMI), these signals require special attention in the routing process.

The highest operating frequency in the flight computer reaches 550 MHz, making the system susceptible to interference from external magnetic fields, as described by $\phi = \frac{d(AB)}{dt}$. Furthermore, these signals can act as sources of EMI, potentially affecting other subsystems. To mitigate these risks, the following routing guidelines are implemented:

1) Maintain minimum spacing between traces and copper pours, as determined by impedance calculations.
2) Surround high-speed traces with ground copper pours to establish shielding.
3) Route signals as continuous, unbranched traces across the PCB to minimize EMI.
4) Keep signal traces as short and parallel as possible to reduce propagation delay mismatches and EMI.



(a) SPI Routing **(b) USB Routing** **(c) Ethernet routing with length tuning**

Special considerations should apply to USB in Fig. 14b and Ethernet differential pairs in Fig. 14c, which require:
1) A consistent trace gap to maintain controlled impedance.
2) Length tuning to ensure matched propagation delay between differential pair signals.

In addition to high-speed digital signals, PWM and analog voltage traces require careful routing due to their susceptibility to EMI, which can degrade system performance. These signals are primarily used for continuity checks in the pyrotechnic module and position definition for actuators. Precautions are taken are taken when routing PWM and analog voltage traces (Fig. 15):
1) Maintain a minimum spacing of 16 mil (0.016 in) to reduce crosstalk
2) Surround traces with ground copper pours to shield them from external magnetic fields
3) Avoid vias and reference plane transitions to maintain signal integrity

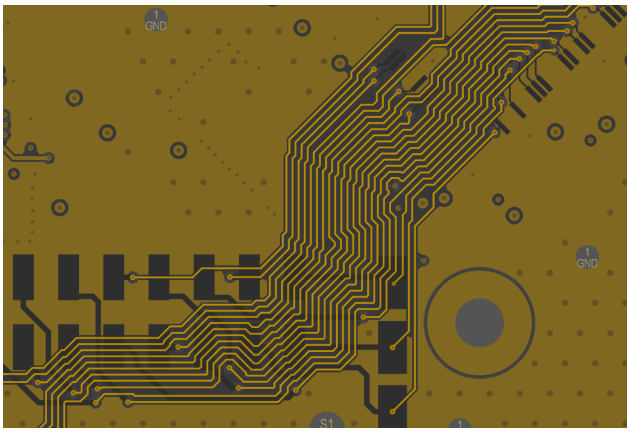


Fig. 15 Analog voltage and PWM signals

C. Redundancy Considerations

Ensuring system reliability is a fundamental aspect of flight computer design. To mitigate potential failures, redundancy measures are implemented across software flashing methods, data storage, and expansion capabilities.

1. Software Flashing Methods

To prevent software deployment failures, flight computer supports multiple flashing methods. Firmware can be uploaded via 2-wire JTAG (Main MCU), 4-wire JTAG (State Estimation MCU), USB, and UART. Among these, 2-wire and 4-wire JTAG are preferred by developers due to their compatibility with widely available debugging tools, such as FTDI-based interfaces, which facilitate efficient software flashing and debugging.

2. Data Storage

Flight computer utilizes both a NOR QSPI flash chip and an SD card for data storage. Due to the relatively low write speed of the SD card—requiring a sector size configuration of 4096 bytes—real-time data is initially stored in the NOR flash chip. At the end of the flight, the stored data is transferred to the SD card to facilitate portability and external analysis.

3. Expansion Capabilities

To enhance system versatility, flight computer includes an Ethernet port, enabling potential integration with additional computing units. This feature allows for expanded connectivity options and provides flexibility for future development and testing scenarios requiring networked communication between multiple systems.

III. Transient Analysis

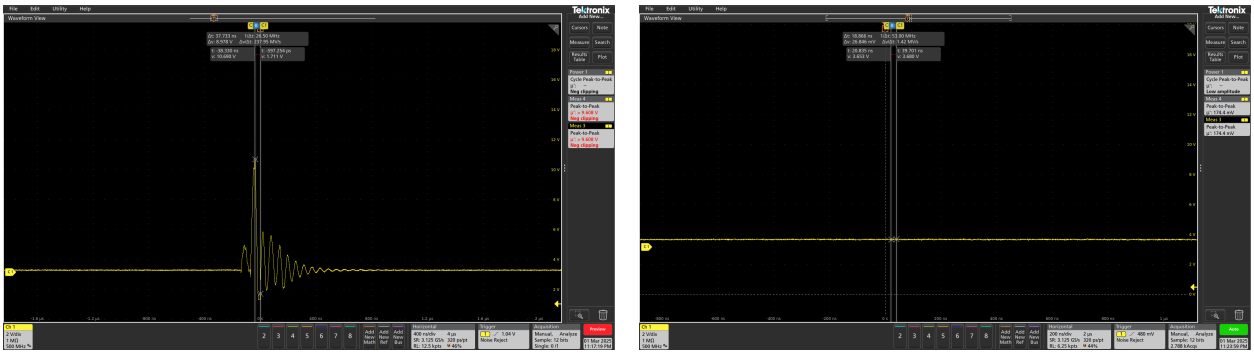
While the avionics hardware is expected and proven to perform as expected during stable states, the transient periods during sudden changes of states also need to be investigated, since they behave vastly differently compared to the stable states.

A. Pyrotechnic Modules Arming Spikes

In order to maximize the factor of safety, last-second arming of the pyrotechnic modules is part of the launch site procedures. This was designed to reduce the chances of misfiring any explosive charges while the crew is still on the pad. However, the transient period between the armed and disarmed state has unexpected voltage spikes (Fig. 16a) up to 10V.

Upon further review, it has been concluded that the gate of the transistor in Fig. 3 has parasitic capacitance. In other words, the gate was not fully regulated and clamped before current was able to rush from the source to the drain of the P-channel transistor, causing a 5-millisecond transient period during which it could potentially ignite the charge.

In order to resolve the issue, a DC-DC regulator was implemented between the power source and the pyrotechnic module, acting as a soft starter. This allows the gate to fully charge by slowly ramping up the voltage. Fig. 16b indicates a negligible transient response, vastly increasing the factor of safety of the avionics system.

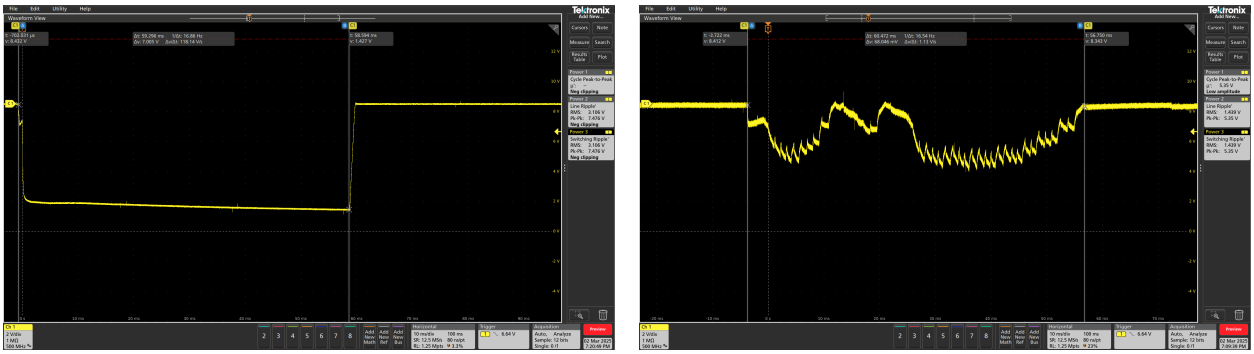


(a) Transient spikes of the arming process **(b) Transient spike with the regulated power source**

Fig. 16 Transient response before and after the implementation of a regulated voltage source

B. Load Transient Response

In case of a drastic actuation of the actuators, the PMS experience a power coma due to large current output for 60 milliseconds (Fig. 17a). In other words, the actuator will lose power for 60 milliseconds if there is a sudden need for large actuation.



(a) Power coma due to large current draw **(b) Transient after capacitor bank implementation**

Fig. 17 Transient response before and after the implementation of a regulated voltage source

In order to tackle the power coma, the study implemented a series of 10 $220\mu F$ electrolytic capacitors (Fig. 18) as an energy reservoir. This allowed achieving the minimum voltage of 5V (the bare minimum operational voltage of the actuators) instead of 2V during the coma (Fig. 17b).

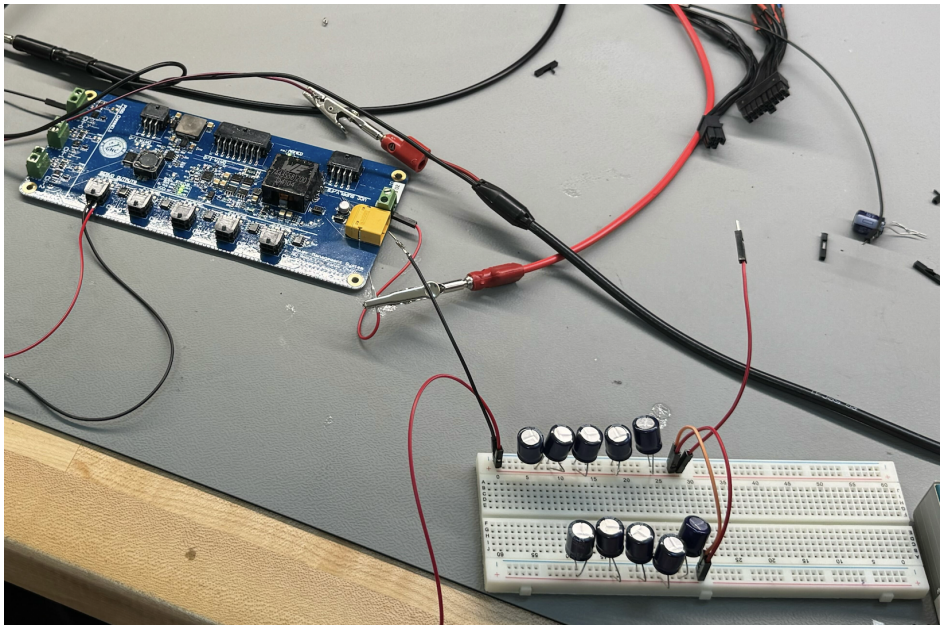


Fig. 18 Electrolytic capacitor bank implementation

IV. Results and Discussion

After completing bench testing of the avionics system, the study proceeded to test it in a real flight environment — a test designed to exceed the requirements of the jet-vane-controlled rocket. The powered-on avionics module was installed inside a Level-2 rocket and launched at a velocity higher than that of the intended vehicle. Prior to the test launch, the L2 rocket remained on the launchpad under direct sunlight for over 30 minutes with the avionics system running. Despite the internal heat buildup within the body tube, the system remained fully operational, thanks to the

advanced cooling mechanism described in section II.A.3. Furthermore, the avionics system successfully withstood the high-G environment and impact shock during landing, further validating its readiness for flight.

V. Conclusion

This study has verified that the compact avionics system is both powerful and robust enough for a high-performance guidance rocket. However, there are still limitations and opportunities for improvement. For example, the DC-DC modules could be redesigned into a multi-phase configuration to improve power efficiency. Additionally, the two existing boards could be further modularized into separate subsystems. Despite these areas for enhancement, it is clear that the flight avionics demonstrate a high level of performance relative to their size. Furthermore, the DC-DC regulated power approach for addressing arming spikes (Section III.A) can serve as a useful reference for other avionics systems.

Looking ahead, the study plans to introduce a power management IC in addition to the current power management system. This enhancement will contribute to a more comprehensive and automated avionics system, further improving the precision and reliability of the system's performance.

Acknowledgments

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